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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,341	02/13/2004	Yi-Hsun Wu	N1085-00190	9607

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EXAMINER	
DANG, ROBERT TRONG	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,341	WU ET AL.	
	Examiner	Art Unit	
	Robert T. Dang	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/13/2004 (2/2).
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Staab et al. (5.610790) Staab discloses the claimed invention at Fig. 1, including, a low capacitance circuit coupled to a pad 101 and ground, (it is low since there is no capacitor and low is a term of degree), a first resistive device 103, comprising a first connection coupled to the pad and a second connection, and a second device 104 coupled to the second connection of the first resistive device and to the ground 105 (see col. 5, lines 5-15). In claim 2, the pad is input power or signal, where "/" means one of input or output meets the claim, or the pad 102 meets the claim. In claims 3-4, the resistor is low impedance 2ohm, where Fig. 7 also meets claim 1, since the resistor 712 coupled to the pad 701 and the pad 711 and to ground, and the second device is 703, with the first and second connections at either end of the resistor. Again, the device is low capacitance since no capacitor is in the circuit and low is a term of degree.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al (6690557) in view of Staab et al (5610790).

As to claims 1-4, Hung discloses in figure 1 a circuit for electrostatic discharge (ESD) protection, comprising: a. a low capacitance ESD protection circuit (102) coupled to an input pad (106) and a ground. However, he fails to disclose a first resistive device, comprising a first connection coupled to the pad and a second connection and a second device coupled to the second connection of the first resistive device and to the ground. Staab discloses in his invention wherein a first resistive device that is low impedance (2 ohms), comprising a first connection coupled to the pad and a second connection and a second device coupled to the second connection of the first resistive device and to the ground (see col. 5, lines 5-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device and add the resistive element between the pad and buffer (consisting of an inverter) in order to reduce the RC delay of signals transmitted from the pad to the buffer.

As to claim 5, Hung discloses in figure 1, wherein the second device comprises an NMOS transistor.

As to claim 6, Hung discloses in figure 1, wherein the source of the NMOS transistor and the gate of the NMOS transistor are coupled to a common junction.

As to claim 7, Hung discloses in figure 1, wherein the common junction is the ground.

As to claims 8-11, Hung discloses in figure 5, a pad (504), buffer circuit, operatively coupled to a voltage terminal and to a ground; an internal circuit (502), operatively coupled to the voltage terminal and to the ground; a low capacitance electrostatic discharge (ESD) protection circuit (508) coupled to the pad and the ground; however, he fails to disclose a first resistive device, comprising a first connection coupled to the pad and a second connection and a second device coupled to the second connection of the first resistive device and to the ground. Staab discloses in his invention wherein a first resistive device that is low impedance (2 ohms), comprising a first connection coupled to the pad and a second connection and a second device coupled to the second connection of the first resistive device and to the ground (see col. 5, lines 5-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device and add the resistive element between the pad and buffer (consisting of an inverter) in order to reduce the RC delay of signals transmitted from the pad to the buffer.

As to claim 12, Hung discloses in figure 1, wherein the second device comprises an NMOS transistor.

As to claim 13, Hung discloses in figure 1, wherein the source of the NMOS transistor and the gate of the NMOS transistor are coupled to a common junction.

As to claim 14, Hung discloses in figure 1, wherein the common junction is the ground.

As to claim 15, Hung discloses in figure 1, wherein: a. the voltage terminal is a V.sub.SS voltage terminal; and b. the first resistive device and the second device effect a current path between the V.sub.SS terminal and the pad.

As to claim 16, Hung discloses the claimed invention except for the NMOS having a width from about 10 .mu.m to about 30 .mu.m with a length from about 0.15 .mu.m to about 0.25 .mu.m. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize an NMOS having a width from about 10 .mu.m to about 30 .mu.m with a length from about 0.15 .mu.m to about 0.25 .mu.m, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233*

As to claims 17-19, Hung discloses in figure 5, a method of protecting an internal circuit from electrostatic discharge (ESD), comprising: a. coupling a functional circuit to an ESD protection circuit; b. coupling the ESD protection circuit to a pad. Although Hung discloses how there is an additional circuit that is used to effect a voltage drop between the pad and the functional circuit to protect thin oxide layers of at least a portion of the functional circuit from damage when an ESD pulse is present at the pad (see col. 2, lines 20-27), nevertheless he does not disclose that it is a resistive element. Staab discloses in his invention wherein operatively coupling an additional circuit (resistive element) intermediate the ESD protection circuit and the functional circuit; and using the additional circuit (resistive element) (2 ohms) as a means to effect a voltage drop between the pad and the functional circuit to protect thin oxide layers of at least a

portion of the functional circuit from damage when an ESD pulse is present at the pad. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device and add the resistive element between the pad and buffer in order to reduce the RC delay of signals transmitted from the pad to the buffer.

As to claim 20, Hung discloses in figure 1, further comprising discharging the ESD pulse to a Vss terminal when the ESD pulse is coupled to the pad (see col. 15, lines 16-22)

As to claim 21, Hung discloses in figure 1, further comprising disabling a current path formed by the coupling of the functional circuit to the ESD protection circuit when no ESD pulse is coupled to the pad (see col. 1, lines 29-42)

As to claim 22, Hung discloses in figure 1, wherein discharging the ESD pulse further comprises punching through a MOS transistor (see col. 1, lines 29-42).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert T. Dang whose telephone number is 571-272-8326. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl D. Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RTD

KARL EASTHOM
SUPERVISORY PATENT EXAMINER